IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Andreev, *et al.*

Serial No.:   10/646,535

Filed: August 22, 2003

Title: SYSTEM AND METHOD FOR EFFICIENTLY TESTING A LARGE
                     RANDOM ACCESS MEMORY SPACE

Grp./A.U.:   2138

Confirmation No.   9860

Examiner: Dipakkumar B. Gandhi

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

> I hereby certify that this correspondence is being electronically filed
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> _Margaret A. Jess_
> (Signature of the person signing the certificate)

Sir:

AMENDMENT UNDER 37 C.F.R. § 1.111

In response to the Examiner's Action mailed February 10, 2006, please amend the above-

identified application as follows:

IN THE SPECIFICATION:

[0031] As stated above, the combinatorial logic 180 employs the portion stored in the pseudo-memory 170 and corresponding data-out bit patterns read from the plurality of RAM arrays ~~160~~ 120 to generate a response bit pattern that matches the probe bit pattern only if all of the data-out bit patterns match the probe bit pattern.

[0031] As stated above, the combinatorial logic 180 employs the portion stored in the pseudo-memory 170 and corresponding data-out bit patterns read from the plurality of RAM arrays 120 to generate a response bit pattern that matches the probe bit pattern only if all of the data-out bit patterns match the probe bit pattern.